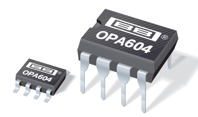
Burr-Brown Products
from Texas Instruments

# OPA604




SBOS019A – JANUARY 1992 – SEPTEMBER 2003

# FET-Input, Low Distortion OPERATIONAL AMPLIFIER

## FEATURES

- **LOW DISTORTION: 0.0003% at 1kHz**
- **LOW NOISE: 10nV/√Hz**
- **HIGH SLEW RATE: 25V/µs**
- **WIDE GAIN-BANDWIDTH: 20MHz**
- **UNITY-GAIN STABLE**
- **WIDE SUPPLY RANGE: $V_S$ = ±4.5 to ±24V**
- **DRIVES 600Ω LOAD**
- **DUAL VERSION AVAILABLE (OPA2604)**

## APPLICATIONS

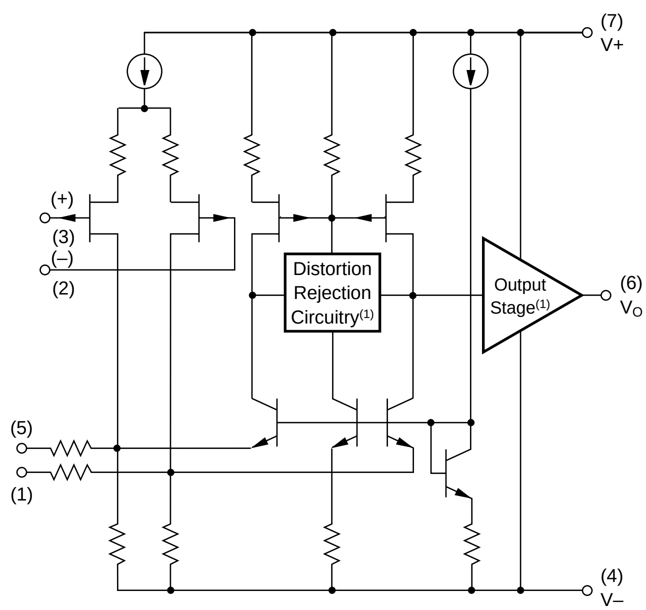
- **PROFESSIONAL AUDIO EQUIPMENT**
- **PCM DAC I/V CONVERTERS**
- **SPECTRAL ANALYSIS EQUIPMENT**
- **ACTIVE FILTERS**
- **TRANSDUCER AMPLIFIERS**
- **DATA ACQUISITION**

## DESCRIPTION

The OPA604 is a FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.




NOTE: (1) Patents Granted: #5053718, 5019789

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TEXAS INSTRUMENTS
www.ti.com

# ELECTRICAL CHARACTERISTICS

$T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

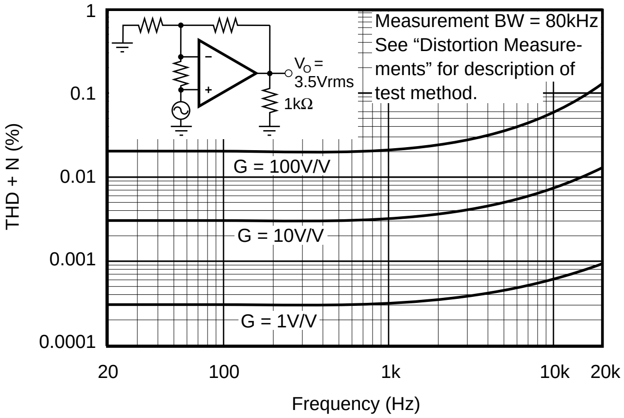
| PARAMETER | CONDITION | OPA604AP, AU | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **OFFSET VOLTAGE** | | | | | |
| Input Offset Voltage | | | ±1 | ±5 | mV |
| Average Drift | | | ±8 | | µV/°C |
| Power Supply Rejection | $V_S$ = ±5 to ±24V | 80 | 100 | | dB |
| **INPUT BIAS CURRENT**(1) | | | | | |
| Input Bias Current | $V_{CM}$ = 0V | | 50 | | pA |
| Input Offset Current | $V_{CM}$ = 0V | | ±3 | | pA |
| **NOISE** | | | | | |
| Input Voltage Noise | | | | | |
| Noise Density: f = 10Hz | | | 25 | | $nV/\sqrt{Hz}$ |
| f = 100Hz | | | 15 | | $nV/\sqrt{Hz}$ |
| f = 1kHz | | | 11 | | $nV/\sqrt{Hz}$ |
| f = 10kHz | | | 10 | | $nV/\sqrt{Hz}$ |
| Voltage Noise, BW = 20Hz to 20kHz | | | 1.5 | | $\mu V_{PP}$ |
| Input Bias Current Noise | | | | | |
| Current Noise Density, f = 0.1Hz to 20kHz | | | 4 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | |
| Common-Mode Input Range | | ±12 | ±13 | | V |
| Common-Mode Rejection | $V_{CM}$ = ±12V | 80 | 100 | | dB |
| **INPUT IMPEDANCE** | | | | | |
| Differential | | | $10^{12}$ \|\| 8 | | Ω \|\| pF |
| Common-Mode | | | $10^{12}$ \|\| 10 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | |
| Open-Loop Voltage Gain | $V_O$ = ±10V, $R_L$ = 1kΩ | 80 | 100 | | dB |
| **FREQUENCY RESPONSE** | | | | | |
| Gain-Bandwidth Product | G = 100 | | 20 | | MHz |
| Slew Rate | $20V_{PP}$, $R_L$ = 1kΩ | 15 | 25 | | V/µs |
| Settling Time: 0.01% | G = –1, 10V Step | | 1.5 | | µs |
| 0.1% | | | 1 | | µs |
| Total Harmonic Distortion + Noise (THD+N) | G = 1, f = 1kHz<br>$V_O$ = 3.5Vrms, $R_L$ = 1kΩ | | 0.0003 | | % |
| **OUTPUT** | | | | | |
| Voltage Output | $R_L$ = 600Ω | ±11 | ±12 | | V |
| Current Output | $V_O$ = ±12V | | ±35 | | mA |
| Short Circuit Current | | | ±40 | | mA |
| Output Resistance, Open-Loop | | | 25 | | Ω |
| **POWER SUPPLY** | | | | | |
| Specified Operating Voltage | | | ±15 | | V |
| Operating Voltage Range | | ±4.5 | | ±24 | V |
| Current | | | ±5.3 | ±7 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –25 | | +85 | °C |
| Storage | | –40 | | +125 | °C |
| Thermal Resistance(2), $\theta_{JA}$ | | | 90 | | °C/W |

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

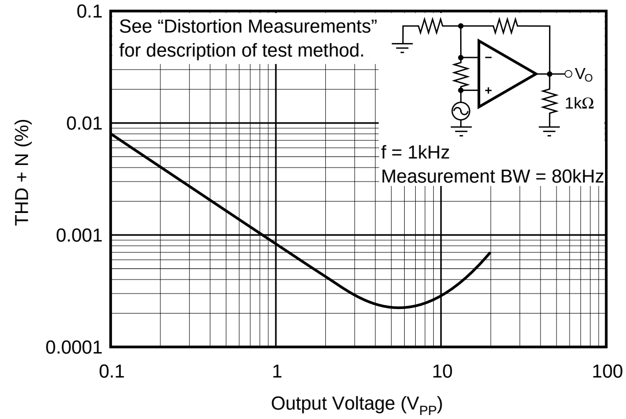
# TYPICAL CHARACTERISTICS

$T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

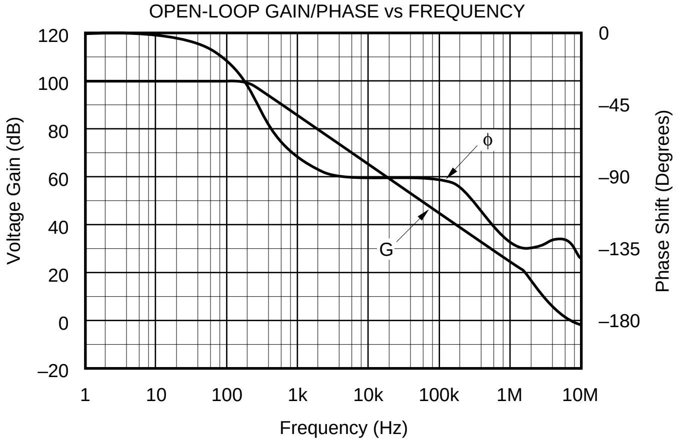
TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY



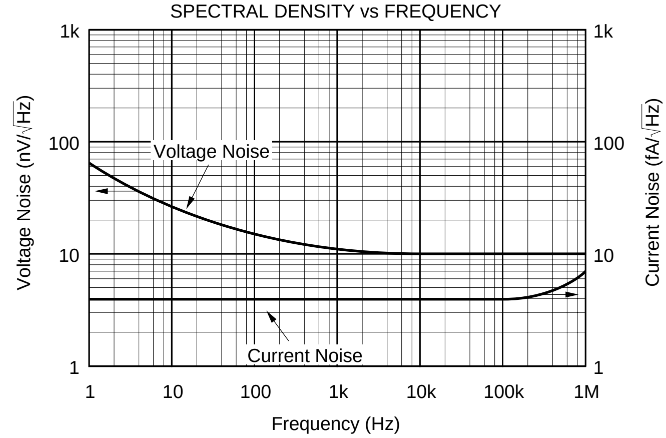

TOTAL HARMONIC DISTORTION + NOISE
vs OUTPUT VOLTAGE



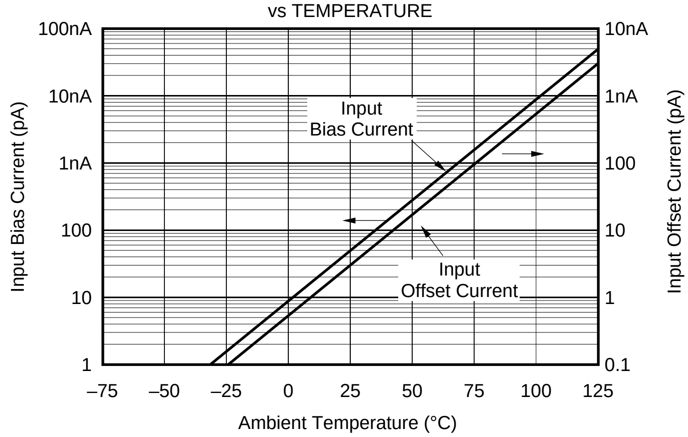

OPEN-LOOP GAIN/PHASE vs FREQUENCY



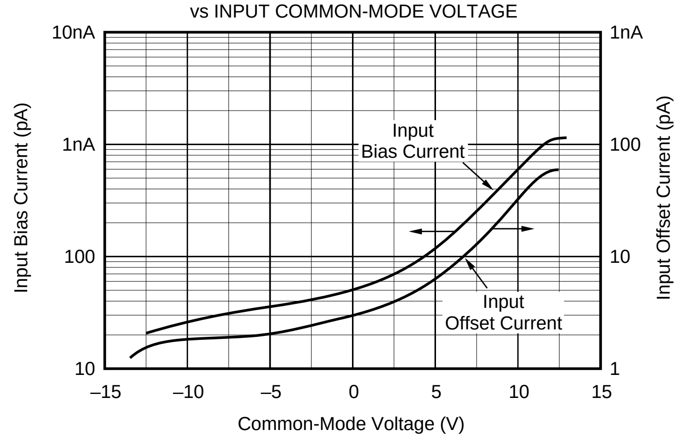

INPUT VOLTAGE AND CURRENT NOISE
SPECTRAL DENSITY vs FREQUENCY




INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



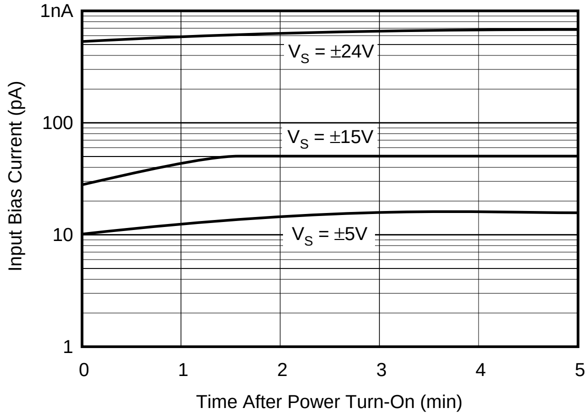

INPUT BIAS AND INPUT OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



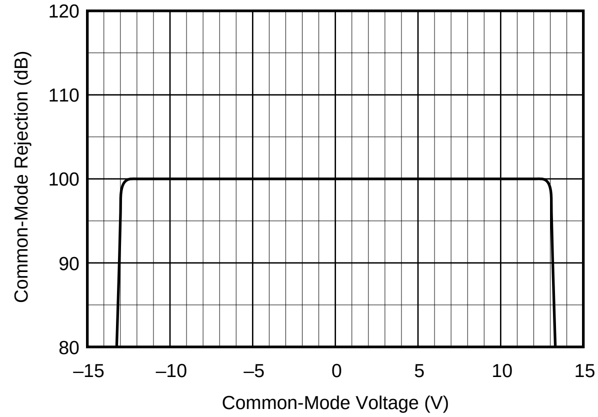
# TYPICAL CHARACTERISTICS (Cont.)

$T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

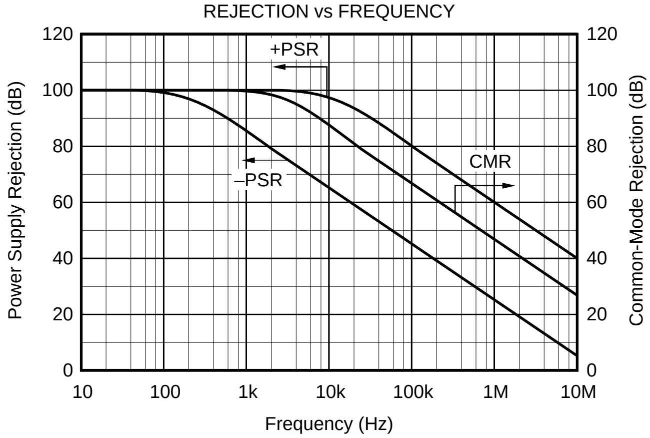
INPUT BIAS CURRENT
vs TIME FROM POWER TURN-ON



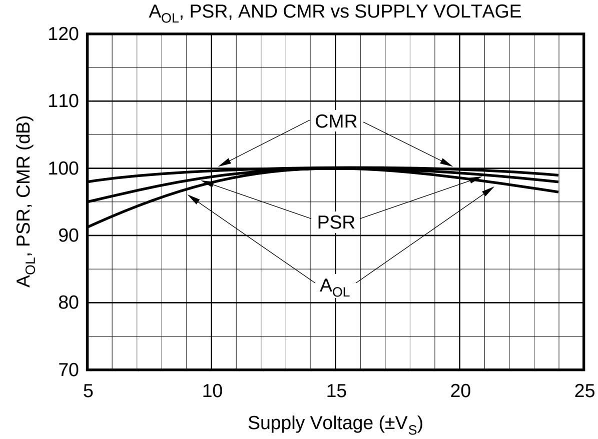

COMMON-MODE REJECTION
vs COMMON-MODE VOLTAGE



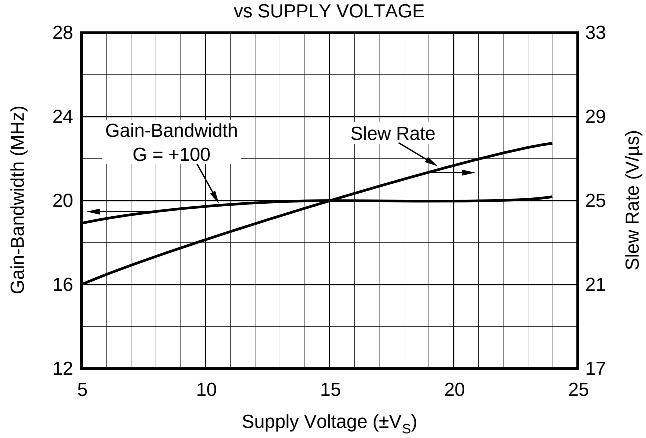

POWER SUPPLY AND COMMON-MODE
REJECTION vs FREQUENCY



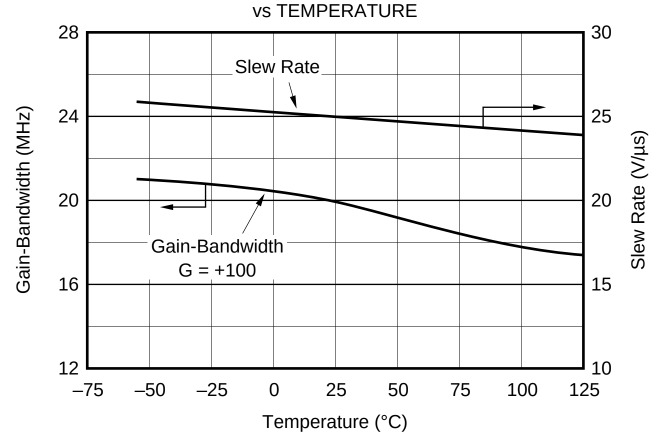

$A_{OL}$, PSR, AND CMR vs SUPPLY VOLTAGE




GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE

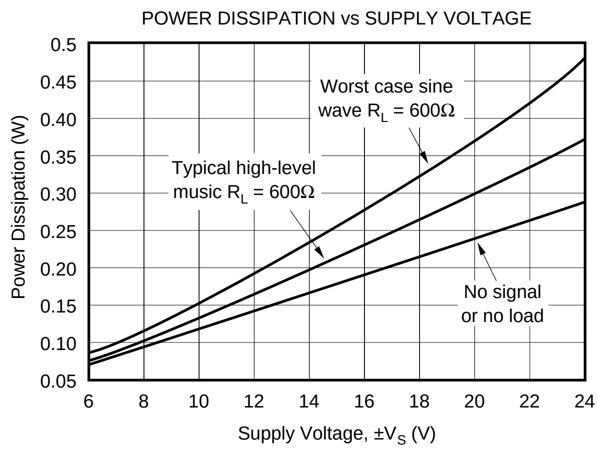


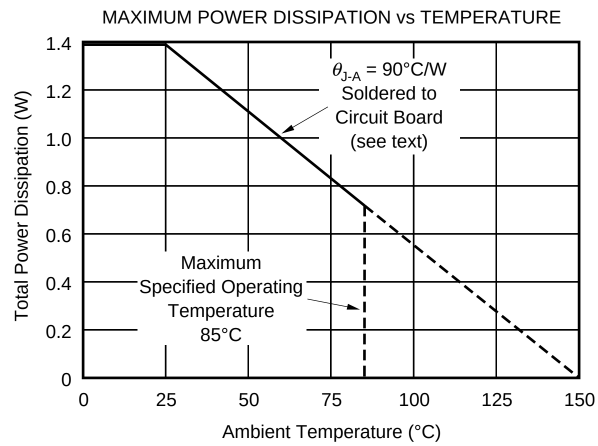

GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



# TYPICAL CHARACTERISTICS (Cont.)

$T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.




# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA604 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. The OPA604 can replace many other amplifiers by leaving the external null circuit unconnected.

The OPA604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases, a 1µF tantalum capacitor at each power supply pin is adequate.

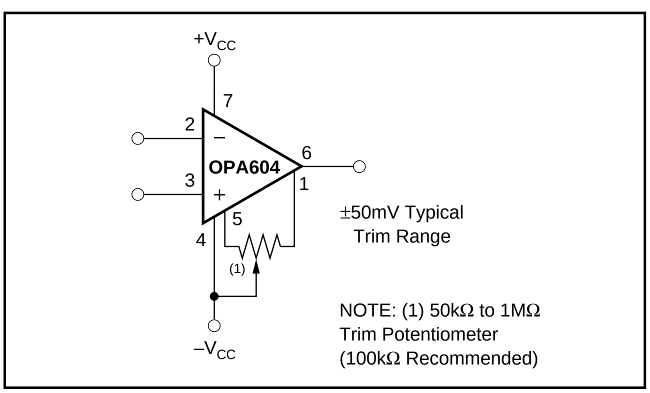



FIGURE 1. Offset Voltage Trim.

## DISTORTION MEASUREMENTS

The distortion produced by the OPA604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 2 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of $R_3$ to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without $R_3$.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

## CAPACITIVE LOADS

The dynamic characteristics of the OPA604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 3 shows various circuits which preserve phase margin with capacitive load. For details of analysis techniques and applications circuits, refer to application bulletin AB-028 (SBOA015) located at www.ti.com.

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reduces
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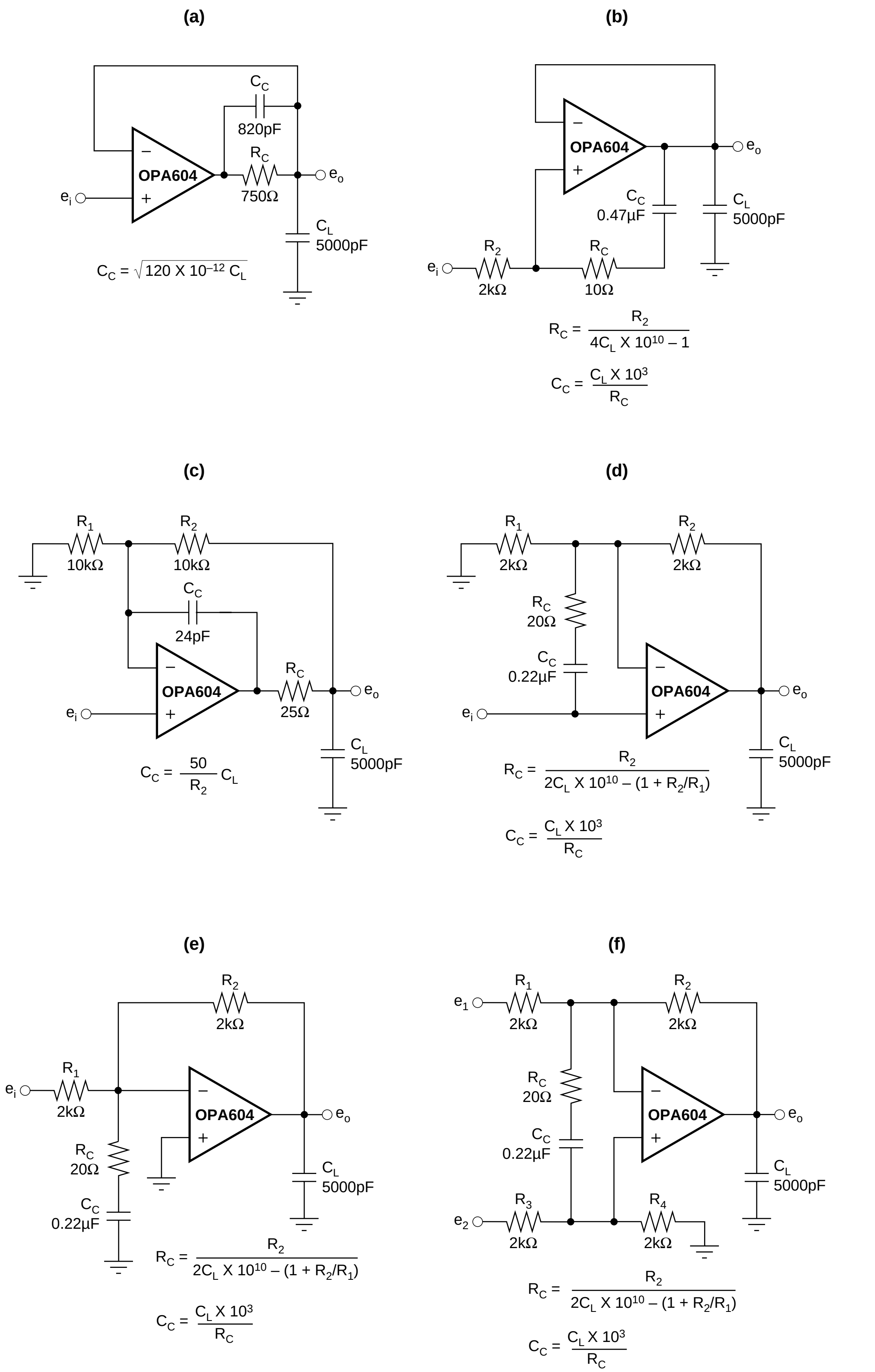



NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 3. Driving Large Capacitive Loads.

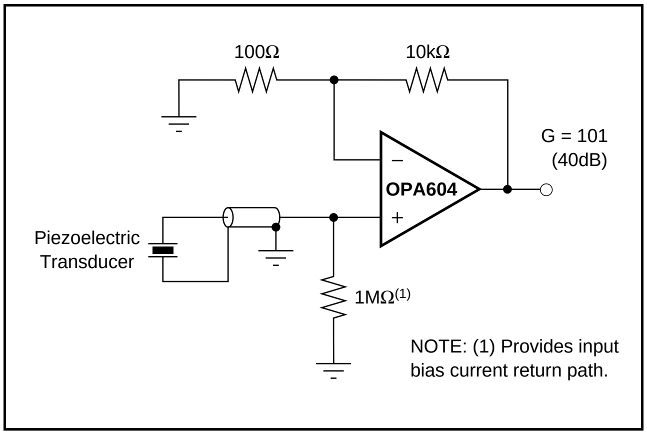



FIGURE 7. High Impedance Amplifier.

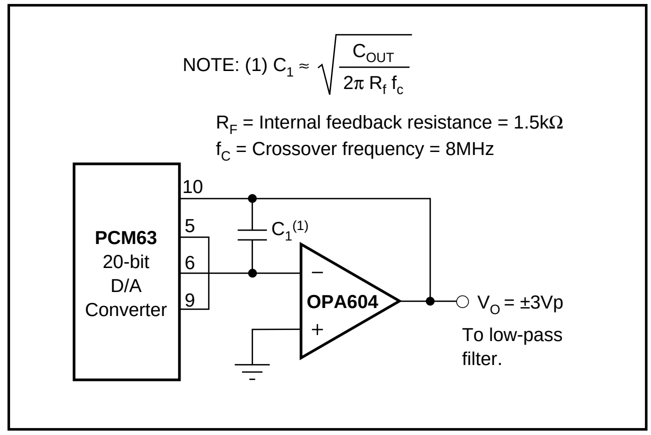



FIGURE 8. Digital Audio DAC I-V Amplifier.

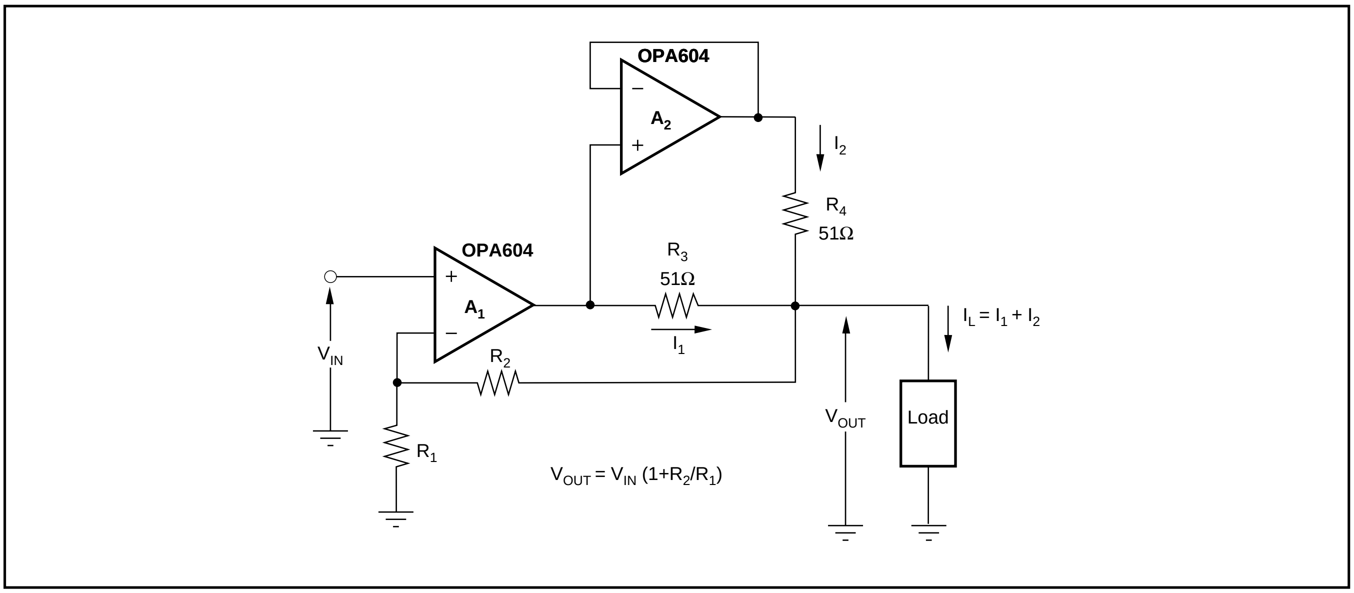



FIGURE 9. Using Two OPA604 Op Amps to Double the Output Current to a Load.

# SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

## SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

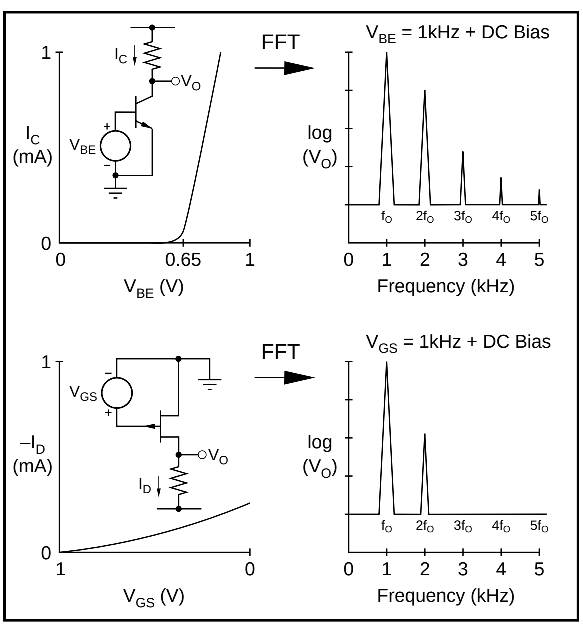
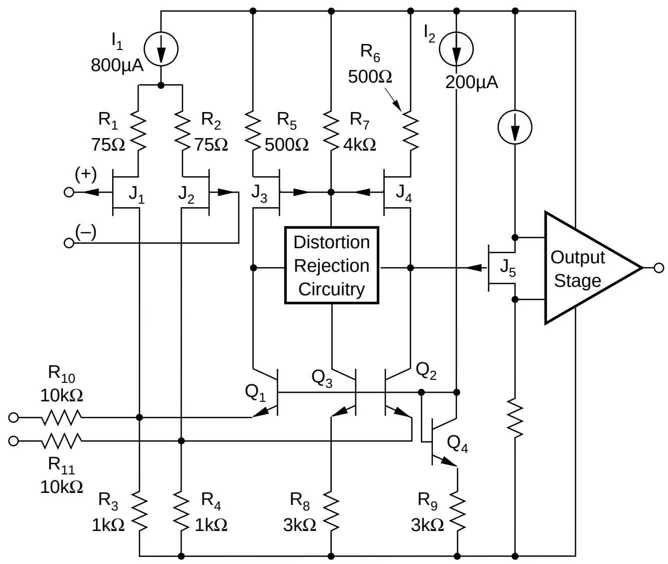



FIGURE 10. I-V and Spectral Response of NPN and JFET.




## THE OPA604 DESIGN

The OPA604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important, and where their transfer characteristics have minimal impact.

The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors $J_1$ and $J_2$ are special large-geometry, P-channel JFETs. Input stage current is a relatively high 800µA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/µs.

The JFET input stage holds input bias current to approximately 50pA or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

The drains of $J_1$ and $J_2$ are cascoded by $Q_1$ and $Q_2$, driving the input stage loads, FETs $J_3$ and $J_4$. Distortion reduction circuitry (patented) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| OPA604AP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| OPA604APG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| OPA604AU | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| OPA604AU/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| OPA604AU/2K5G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| OPA604AUE4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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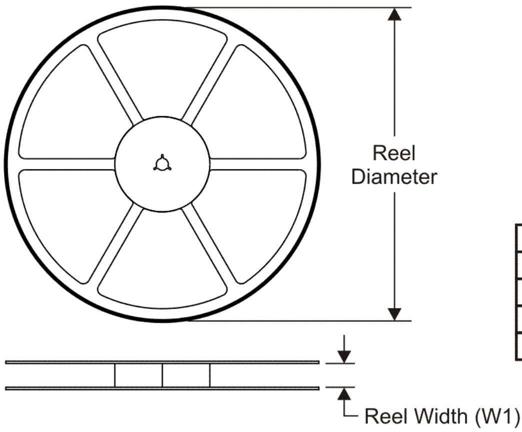
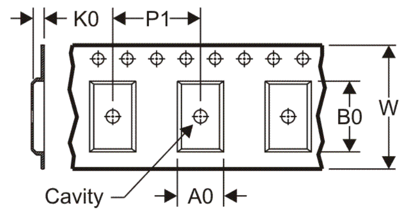
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

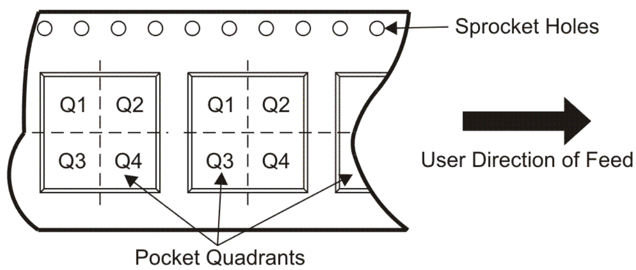



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

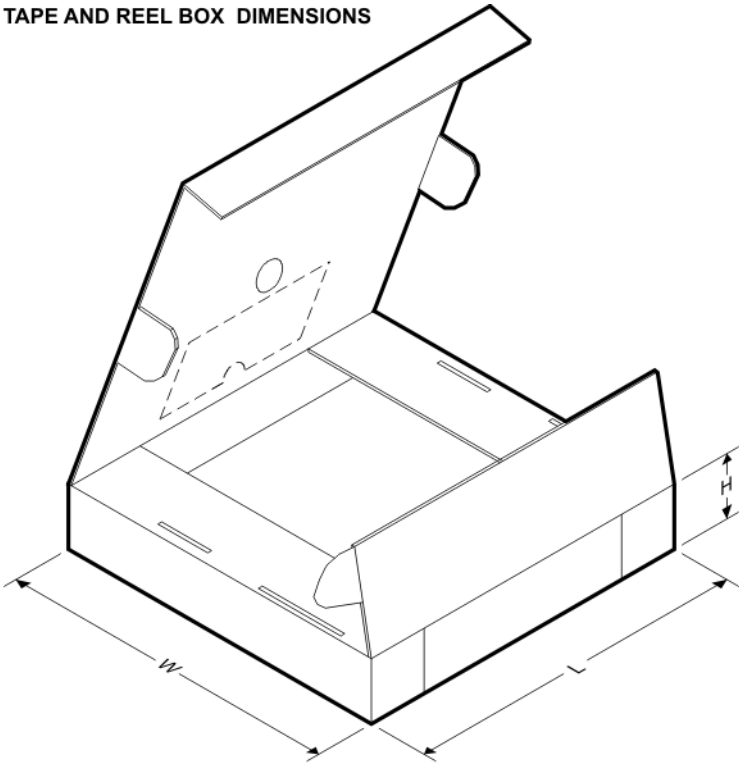
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA604AU/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

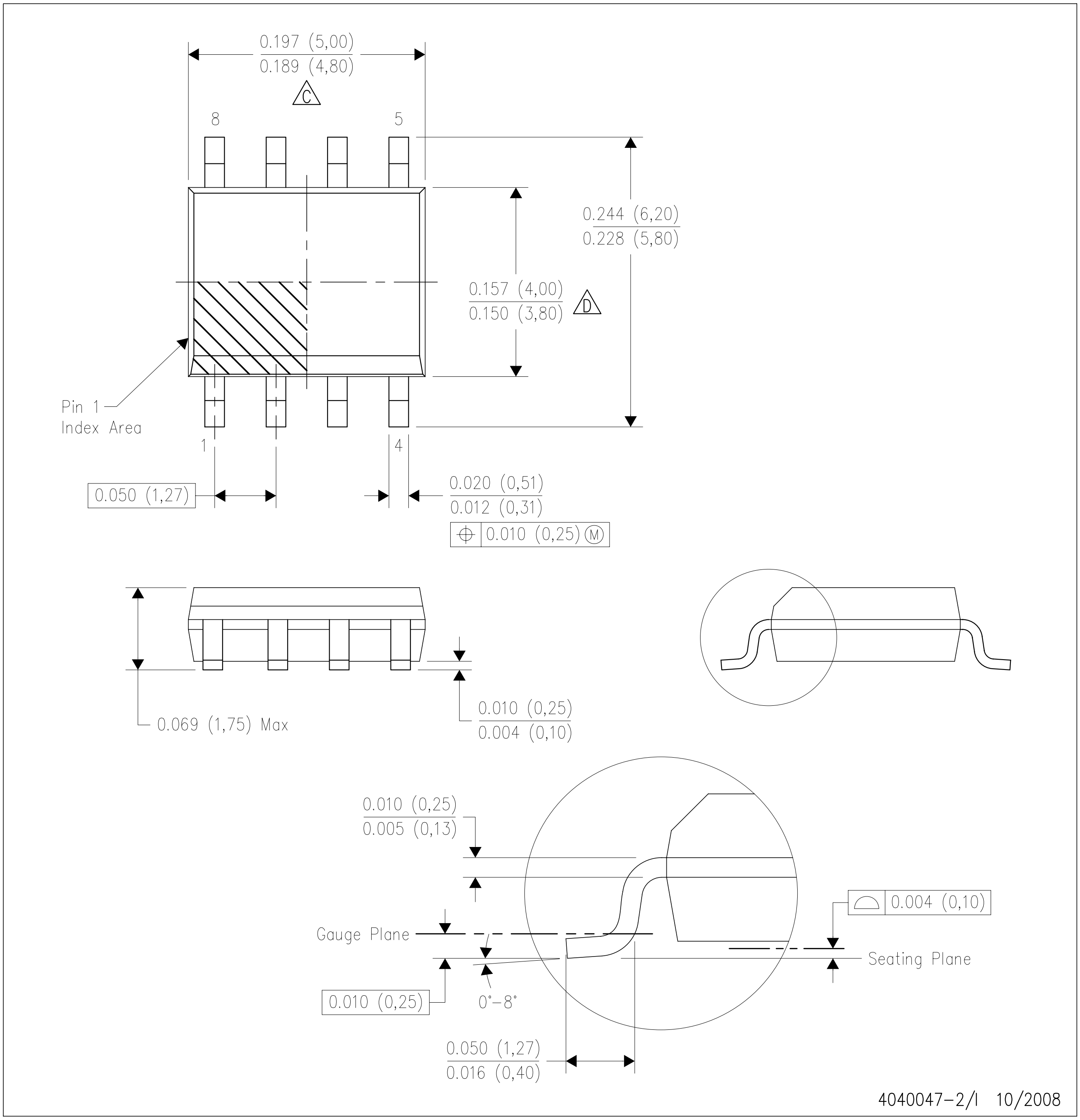
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

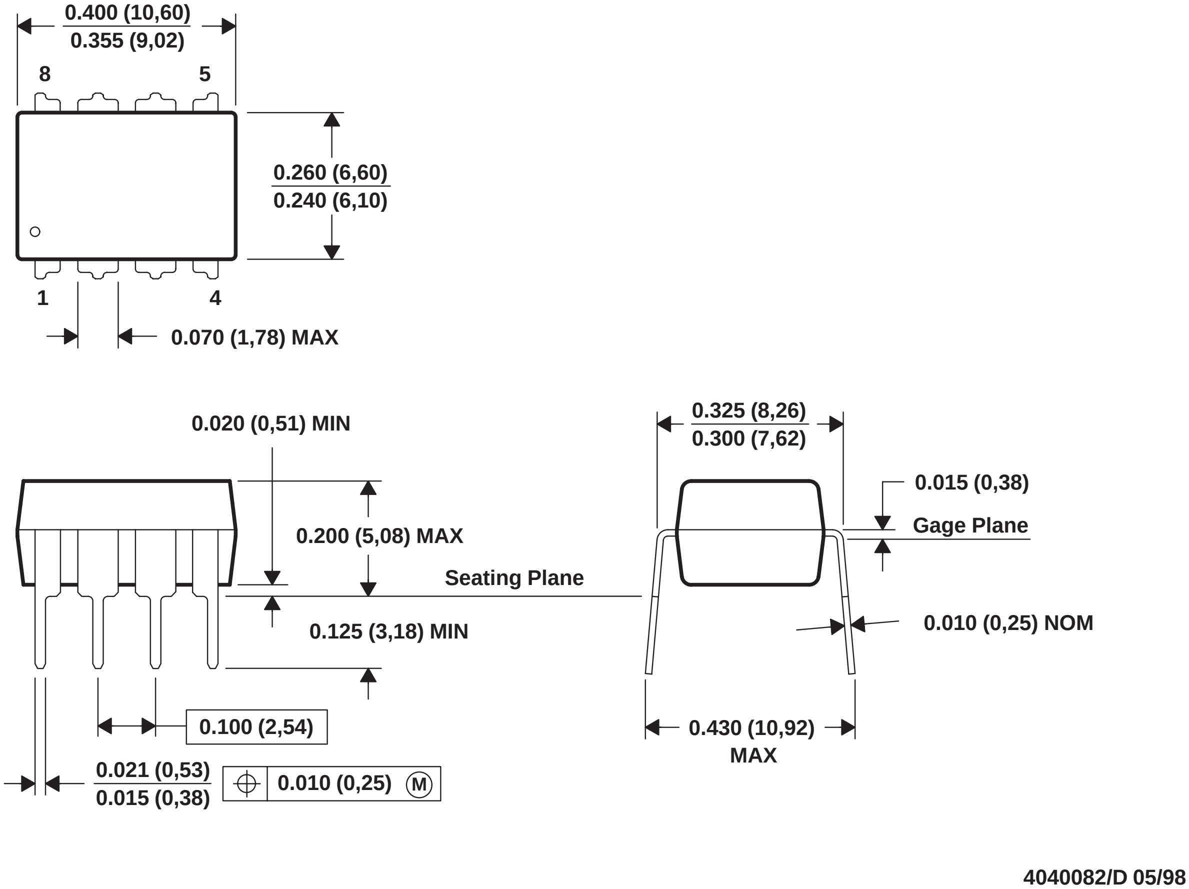
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA604AU/2K5 | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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